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the running time of the optimizer, making **optimized code** available sooner. Another side effect of
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80%

Paul Beckett , Andrew Jennings

Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture - Volume 6 January 2002
Volume 24 Issue 3

At the nanometer scale, the focus of micro-architecture will move from processing to communication. Most general computer architectures to date have been based on a "stored program" paradigm that differentiates between memory and processing and relies on communication over busses and other (relatively) long distance mechanisms.

Nanometer-scale electronics --- nanoelectronics - promises to fundamentally change the ground-rules. Processing will be cheap and plentiful, interconnection expensive but ...

2 [Instruction path coprocessors](#)

80%

Yuan Chou , John Paul Shen

ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture May 2000
Volume 28 Issue 2

This paper presents the concept of an Instruction Path Coprocessor (I-COP), which is a programmable on-chip coprocessor, with its own mini-instruction set, that operates on the core processor's instructions to transform them into an internal format that can be more efficiently executed. It is located off the critical path of the core processor to ensure that it does not negatively impact the core processor's cycle time or pipeline depth. An I-COP is highly versatile and can be used ...

3 [Simulation and architecture evaluation: Vector vs. superscalar and VLIW architectures for embedded multimedia benchmarks](#)

77%

Christoforos Kozyrakis , David Patterson

Proceedings of the 35th annual ACM/IEEE international symposium on

Microarchitecture November 2002

Multimedia processing on embedded devices requires an architecture that leads to high performance, low power consumption, reduced design complexity, and small code size. In this paper, we use EEMBC, an industrial benchmark suite, to compare the VIRAM vector architecture to superscalar and VLIW processors for embedded multimedia applications. The comparison covers the VIRAM instruction set, vectorizing compiler, and the prototype chip that integrates a vector processor with DRAM main memory. We de ...

4 Multithreading and value prediction: Dynamic speculative precomputation 77%

4 Jamison D. Collins , Dean M. Tullsen , Hong Wang , John P. Shen

Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture December 2001

A large number of memory accesses in memory-bound applications are irregular, such as pointer dereferences, and can be effectively targeted by thread-based prefetching techniques like Speculative Precomputation. These techniques execute instructions, for example on an available SMT thread context, that have been extracted directly from the program they are trying to accelerate. Proposed techniques typically require manual user intervention to extract and optimize instruction sequences. This page ...

5 Attacking the semantic gap between application programming languages and configurable hardware 77%

4 Greg Snider , Barry Shackleford , Richard J. Carter

Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays February 2001

It is difficult to exploit the massive, fine-grained parallelism of configurable hardware with a conventional application programming language such as C, Pascal or Java. The difficulty arises from the mismatch between the synchronous, concurrent processing capability of the hardware and the expressiveness of the language-the so-called "semantic gap." We attack this problem by using a programming model matched to the hardware's capabilities that can be implemented in any (unmodified) objec ...

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4 Paul Frenger

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Design Automation Conference, 2002. Proceedings. 39th , 10-14 June
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5 Optimization for a superscalar out-of-order machine

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